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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,674	11/24/2003	Ming-Hsuan Chang	MR3029-82	1648

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,674	CHANG, MING-HSUAN	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-15* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 09/27/2004 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 1-15 in the Paper filed 09/27/2004 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 11/24/2003 is acceptable.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "36" has been used to designate both "a semiconductor layer" and "a sixth conducting structure." Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, claim 6's claimed transistor comprising a first conducting structure upon a substrate; a second conducting structure upon said substrate, with the projection of said second conducting structure onto said substrate intersecting the projection of said first conducting structure onto said substrate; a third conducting structure upon said substrate contacting with said first conducting structure, with the projection of said third conducting structure onto said substrate separated from said projection of said second conducting structure onto said substrate; a fourth conducting structure upon said substrate contacting with said second conducting structure, with the projection of said fourth conducting structure onto said substrate separated from said projection of said first conducting structure onto said substrate, and said fourth conducting structure onto said substrate intersecting the projection of said third conducting structure onto said substrate; and a fifth conducting structure upon said substrate, with the projection of said fifth conducting structure onto said substrate at least partly overlapping said projection of said fourth conducting structure onto said substrate and separated from said projection of said third, said first, and said second conducting structure onto said substrate, while said projection of said fifth conducting structure onto said substrate not completely inside said projection of said fourth conducting structure onto said substrate, said projection of said fifth conducting struc-

ture onto said substrate not contacting with the end of said projection of said fourth conducting structure onto said substrate not contacting with said second conducting structure, and wherein the opposite two sides of said projection of said fourth conducting structure onto said substrate passed by said projection of said fifth conducting structure onto said substrate approximately parallel to one another at and near the intersecting area of said projection of said fourth and said fifth conducting structure must be shown, or the feature(s) canceled from the claim(s). Each element of the claim 6 transistor must be drawn, as well as each claimed relationship between claimed elements, or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and in-

formed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Priority

5. Applicants have made no claim for priority.

Information Disclosure Statement

6. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 7-15 are rejected under 35 U.S.C. 102(b) as being anticipated by MOROZUMI (4,600,274).

With regard to claims 1-4 and 7-9, Morozumi discloses a transistor with a first conducting structure, for example, signal/data line 43, upon a substrate 40; a second conducting structure, for example scanning/gate line 44, upon said substrate 40, with the projection of said second conducting structure 44 onto said substrate 40 intersecting the projection of said first conducting structure 43 onto said substrate 40; a third conducting structure, for example source 53, upon said substrate 40 contacting with said first conducting structure 43, with the projection of said third conducting structure 53 onto said substrate 40 separated from said projection of said second conducting structure 44 onto said substrate 40; a fourth conducting structure, for example gate 50, upon said substrate 40 contacting with said second conducting structure 44, with the projection of said fourth conducting structure 50 onto said substrate 40 separated from said projection of said first conducting structure 43 onto said substrate 40, and said fourth conducting structure 50 onto said substrate 40 intersecting the projection of said third conducting

structure 53 onto said substrate 40; and a fifth conducting structure, for example drain 54, upon said substrate 40, with the projection of said fifth conducting structure 54 onto said substrate 40 at least partly overlapping said projection of said fourth conducting structure 50 onto said substrate 40 and separated from said projection of said third 53, said first 43, and said second conducting structure 44 onto said substrate 40; a semi-conductor layer, for example channel region 55, upon said substrate 40 and electrically coupling with said third 53 and said fifth conducting structure 54 with the projection of said semiconductor layer 55 onto said substrate 40 completely inside said projection of said fourth conducting structure 50 onto said substrate 40; wherein said projection of said fifth 54 and said second conducting structure 44 onto said substrate 40 are on the opposite sides of said projection of said third conducting structure 53 onto said substrate 40, said projection of said fifth conducting structure 54 onto said substrate 40 does not contact with the end of said projection of said fourth conducting structure 50 onto said substrate 40 not contacting with said second conducting structure 44, said projection of said fifth conducting structure 54 onto said substrate 40 completely inside said projection of said fourth conducting structure 50 onto said substrate 40, wherein the opposite two sides of said projection of said fifth conducting structure 54 onto said substrate 40 passed by said projection of said fourth conducting structure 50 onto said substrate 40 approxi-mately parallel to one another at and near the intersecting area of said projection of said fourth 50 and said fifth conducting structure 54 and said projection of said fifth 54 and said fourth conducting structure 50 onto said substrate 40 being approximately parallel-

ograms (rectangles are parallelograms). Note figures 4a, 4c, and column 4 lines 15-36 and 54-68 of Morozumi. With regard to claims 10-15, Morozumi discloses a transistor with a first conducting structure, for example, signal/data line 43, upon a substrate 40; a second conducting structure, for example scanning/gate line 44, upon said substrate 40, with the projection of said second conducting structure 44 onto said substrate 40 intersecting the projection of said first conducting structure 43 onto said substrate 40; a third conducting structure, for example source 53, upon said substrate 40 contacting with said first conducting structure 43, with the projection of said third conducting structure 53 onto said substrate 40 separated from said projection of said second conducting structure 44 onto said substrate 40; a fourth conducting structure, for example gate 50, upon said substrate 40 contacting with said second conducting structure 44, with the projection of said fourth conducting structure 50 onto said substrate 40 separated from said projection of said first conducting structure 43 onto said substrate 40, and said fourth conducting structure 50 onto said substrate 40 intersecting the projection of said third conducting structure 53 onto said substrate 40; and a fifth conducting structure, for example drain 54, upon said substrate 40, with the projection of said fifth conducting structure 54 onto said substrate 40 at least partly overlapping said projection of said fourth conducting structure 50 onto said substrate 40 and separated from said projection of said third 53, said first 43, and said second conducting structure 44 onto said substrate 40; a semiconductor layer, for example channel region 55, upon said substrate 40 and electrically coupling with said third 53 and said fifth conducting structure 54 with the

projection of said semiconductor layer 55 onto said substrate 40 completely inside said projection of said fourth conducting structure 50 onto said substrate 40; wherein said projection of said fifth 54 and said second conducting structure 44 onto said substrate 40 are on the opposite sides of said projection of said third conducting structure 53 onto said substrate 40, said projection of said fifth conducting structure 54 onto said substrate 40 does not contact with the end of said projection of said fourth conducting structure 50 onto said substrate 40 not contacting with said second conducting structure 44, said projection of said fifth conducting structure 54 onto said substrate 40 completely inside said projection of said fourth conducting structure 50 onto said substrate 40, while said projection of said fifth conducting structure 54 onto said substrate 40 not completely inside said projection of said fourth conducting structure 50 onto said substrate 40, said projection of said fifth conducting structure 54 onto said substrate 40 not contacting with the end of said projection of said fourth conducting structure 50 onto said substrate 40 not contacting with said second conducting structure 44 and the opposite two sides of said projection of said fourth conducting structure 50 onto said substrate 40 passed by said projection of said fifth conducting structure 54 onto said substrate 40 approximately parallel to one another at and near the intersecting area of said projection of said fourth 50 and said fifth conducting structure 54, and, further, wherein the opposite two sides of said projection of said fifth conducting structure 54 onto said substrate 40 passed by said projection of said fourth conducting structure 50 onto said substrate 40 approximately parallel to one another at and near the intersecting area of said projection of said

fourth 50 and said fifth conducting structure 54 and said projection of said fifth 54 and said fourth conducting structure 50 onto said substrate 40 being approximately parallelograms. Note figures 4a, 4c, and column 4 lines 15-36 and 54-68 of Morozumi.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
10/04

Minhloan Tran
Primary Examiner
Art Unit 2826